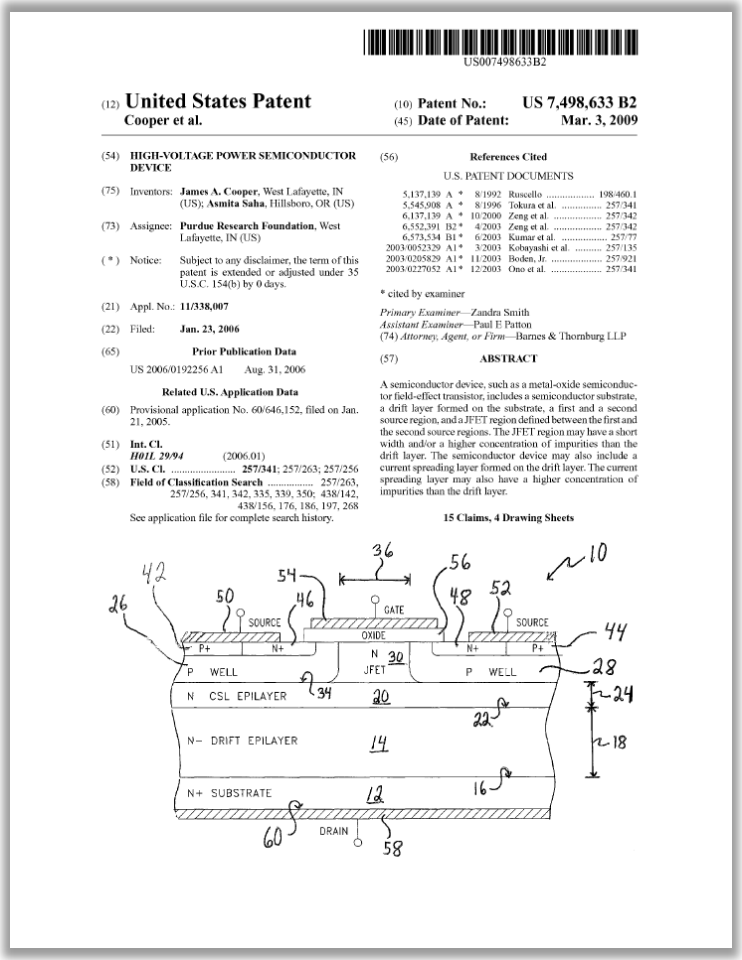
EXHIBIT C



US007498633B2

(12) **United States Patent**
Cooper et al.

(10) **Patent No.: US 7,498,633 B2**
(45) **Date of Patent: Mar. 3, 2009**

(54) **HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**

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(73) Assignee: **Purdue Research Foundation**, West Lafayette, IN (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/338,007**

(22) Filed: **Jan. 23, 2006**

(65) **Prior Publication Data**

US 2006/0192256 A1 Aug. 31, 2006

Related U.S. Application Data

(60) Provisional application No. 60/646,152, filed on Jan. 21, 2005.

(51) **Int. Cl.**
H01L 29/94 (2006.01)

(52) **U.S. Cl.** **257/341**; 257/263; 257/256

(58) **Field of Classification Search** 257/263, 257/256, 341, 342, 335, 339, 350; 438/142, 438/156, 176, 186, 197, 268

See application file for complete search history.

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(57) **ABSTRACT**

A semiconductor device, such as a metal-oxide semiconductor field-effect transistor, includes a semiconductor substrate, a drift layer formed on the substrate, a first and a second source region, and a JFET region defined between the first and the second source regions. The JFET region may have a short width and/or a higher concentration of impurities than the drift layer. The semiconductor device may also include a current spreading layer formed on the drift layer. The current spreading layer may also have a higher concentration of impurities than the drift layer.

15 Claims, 4 Drawing Sheets

Title: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

Priority Date: Jan. 21, 2005

Filed Date: Jan. 23, 2006

Issued Date: Mar. 03, 2009

Expiration Date: Jan. 23, 2026

Inventors: James A. Cooper; Asmita Saha

Exemplary Claim: 9

Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:
a **(SUB) silicon-carbide substrate**;
a **(DL) drift semiconductor layer** formed on a **(FS) front side** of the **(SUB) semiconductor substrate**;
a **(FS) first source region**;
a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;
a **(FBC) plurality of first base contact regions** defined in the **(d) first source region**,
(FBC) each of the plurality of first base contact regions being spaced apart from each other in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;
a **(SS) second source region**;
a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;
a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**,
(SBC) each of the plurality of second base contact regions being spaced apart from each other in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and
a **(JF) JFET region defined between** the **(FS) first source region** and the **(SS) second source region**,
the **(JF) JFET region having a width less than about three micrometers**.

Claim 9

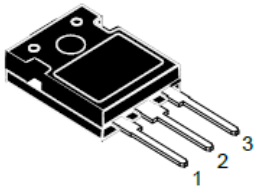
A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

life.augmented

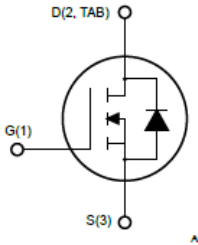
SCTW90N65G2V

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ., T_J = 25 °C) in an HiP247 package



HiP247



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability (T_J = 200 °C)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

U.S. Patent No. 7,498,633 – STMicroelectronics SCTW90N65G2V

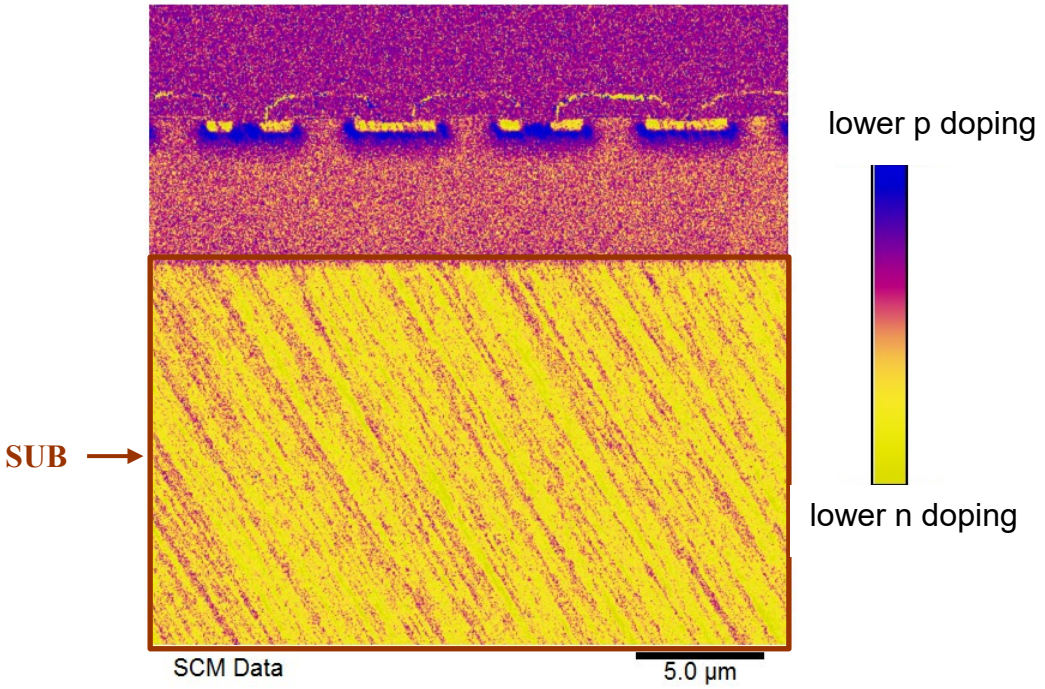
Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

Note: Source and drain regions are produced by ion implantation in silicon carbide, rather than thermal diffusion, because thermal diffusion is too slow to be practical in silicon carbide. So it is expected that the source and drain regions are created by an ion implantation process, hence the double-implanted limitation would be met.

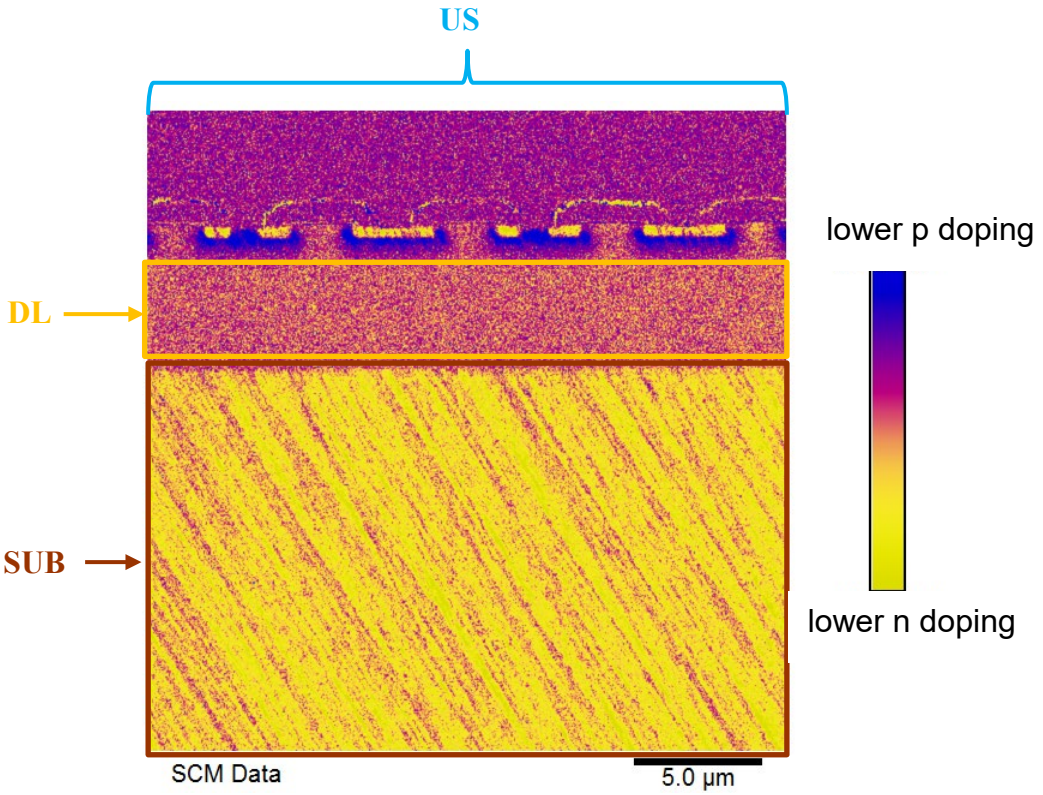
Claim 9

a **(SUB) silicon-carbide substrate**;



Claim 9

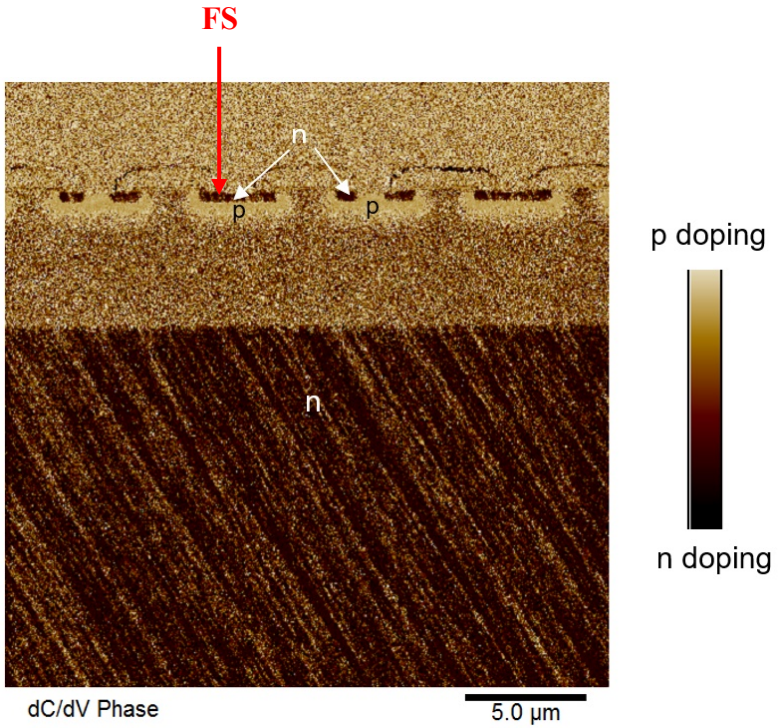
a **(DL) drift semiconductor layer** formed on a **(US) front side** of the **(SUB) semiconductor substrate**;



U.S. Patent No. 7,498,633 – STMicroelectronics SCTW90N65G2V

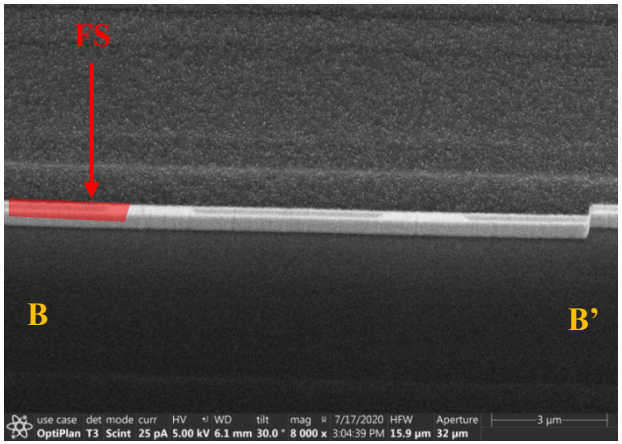
Claim 9

a **(FS) first source region**;

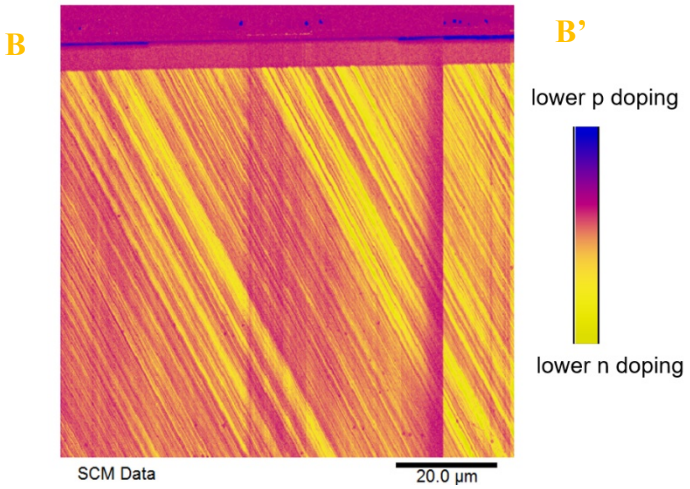


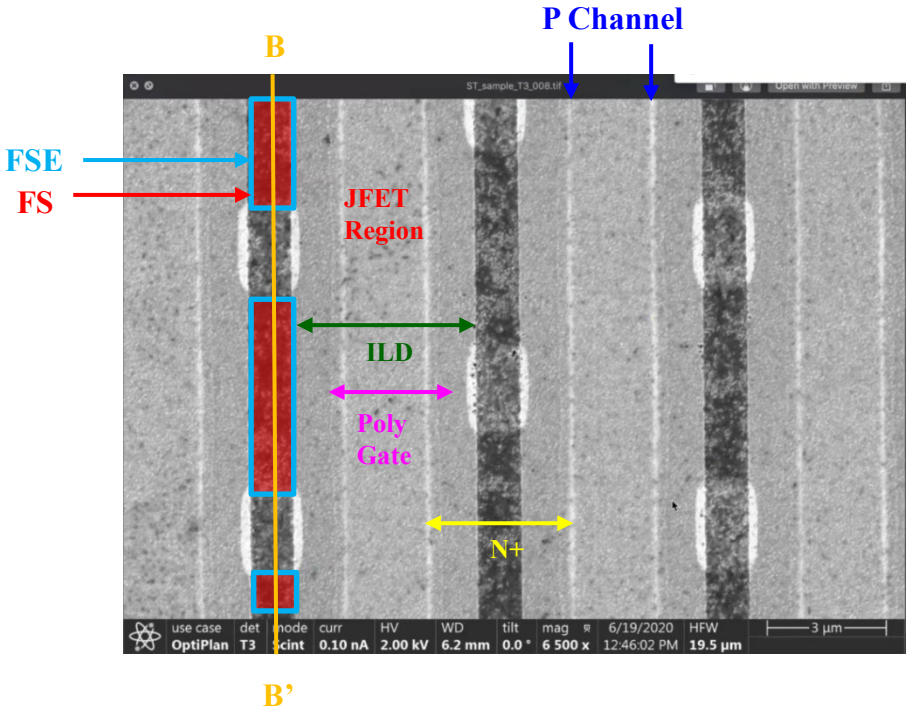
Claim 9

a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;



Note: The cross-section SEM SEPC above has been polished down to the silicon carbide.



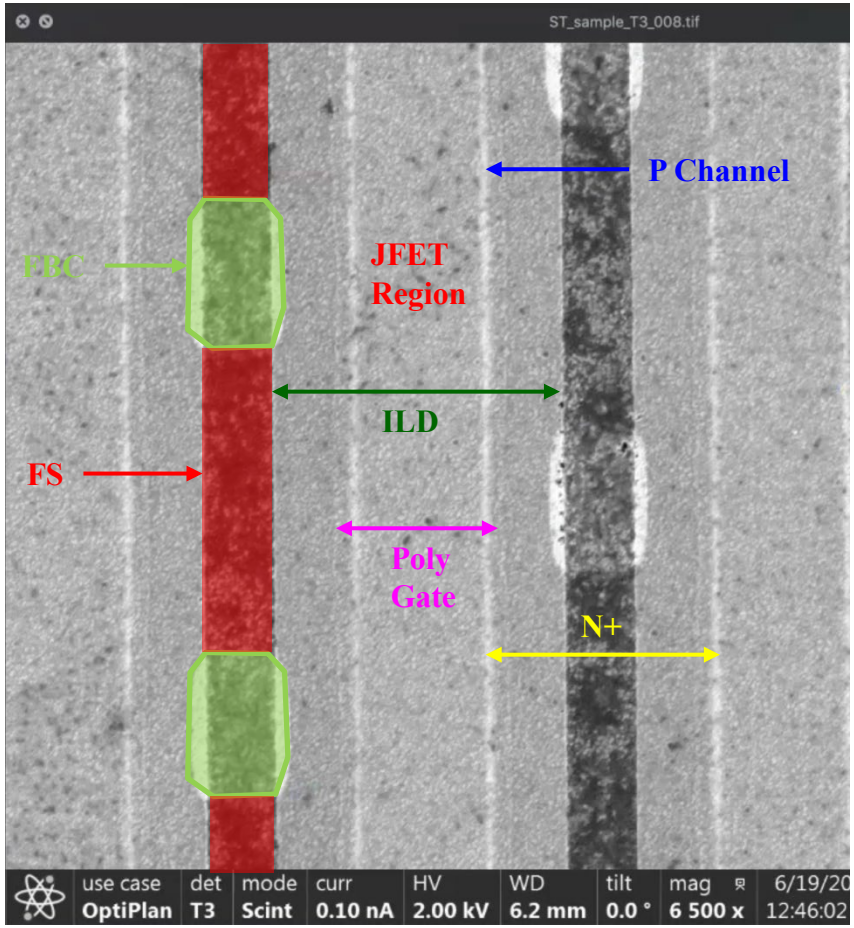


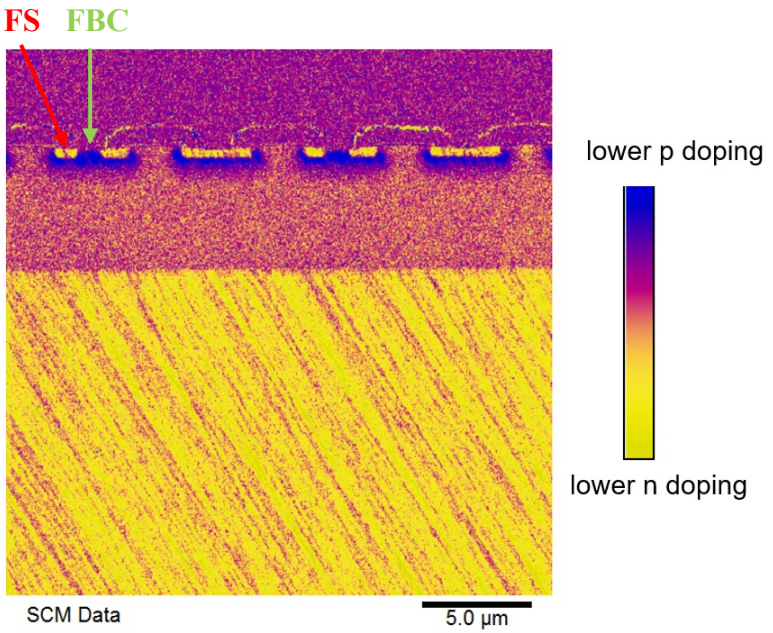
Cut Line for Cross Section

Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

a **(FBC) plurality of first base contact regions** defined in the **(FS) first source region**,

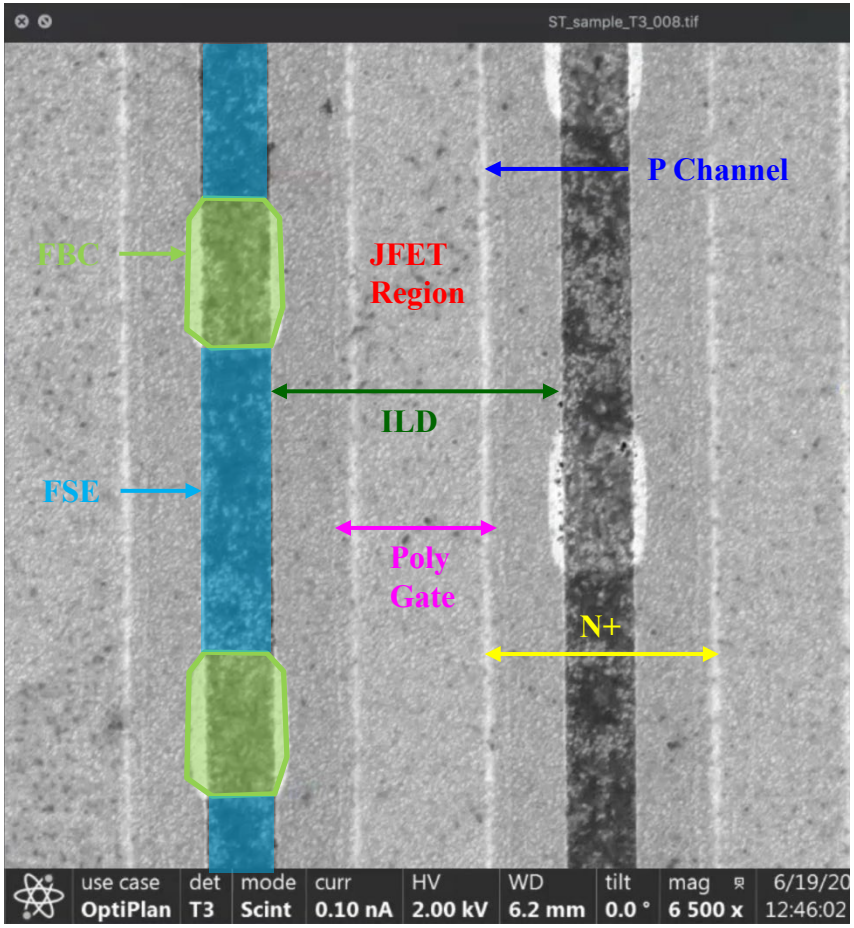


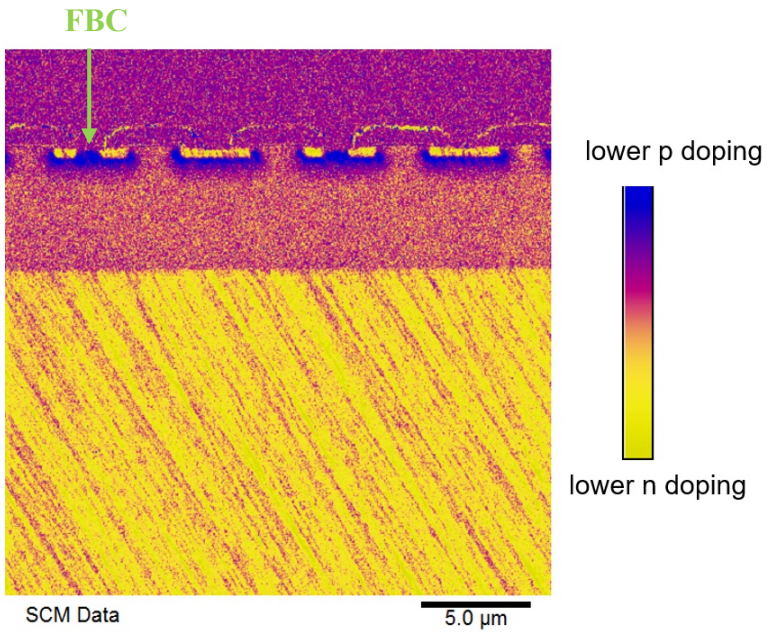


Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

(FBC) each of the plurality of first base contact regions being spaced apart from each other in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;

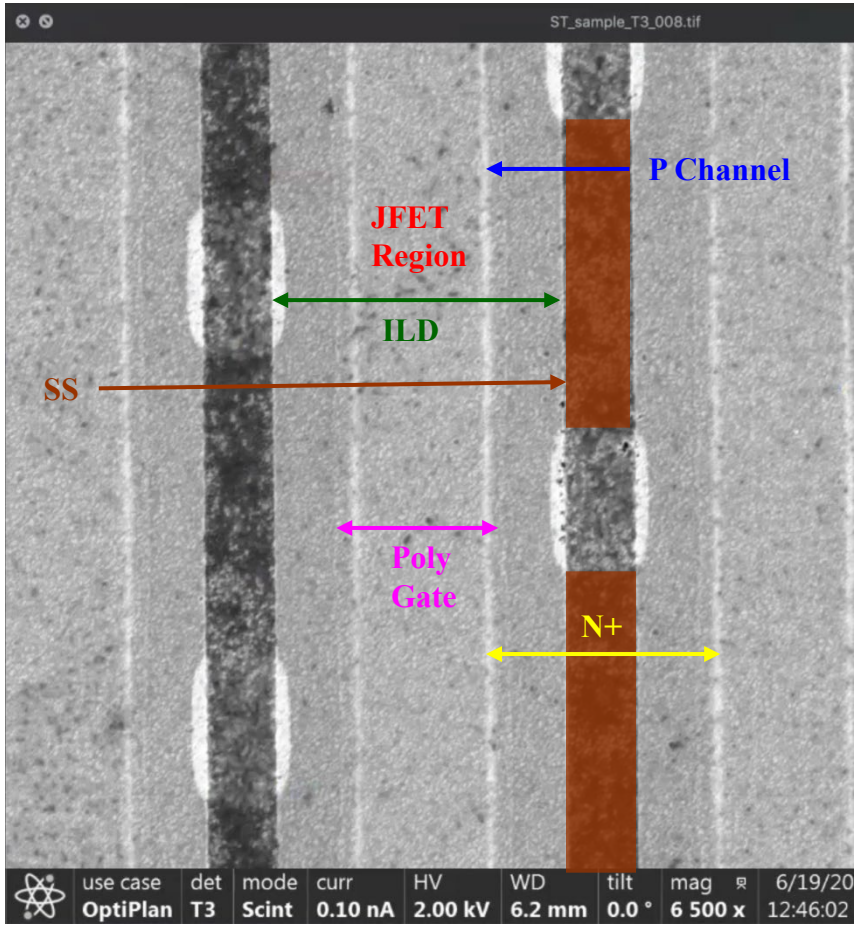


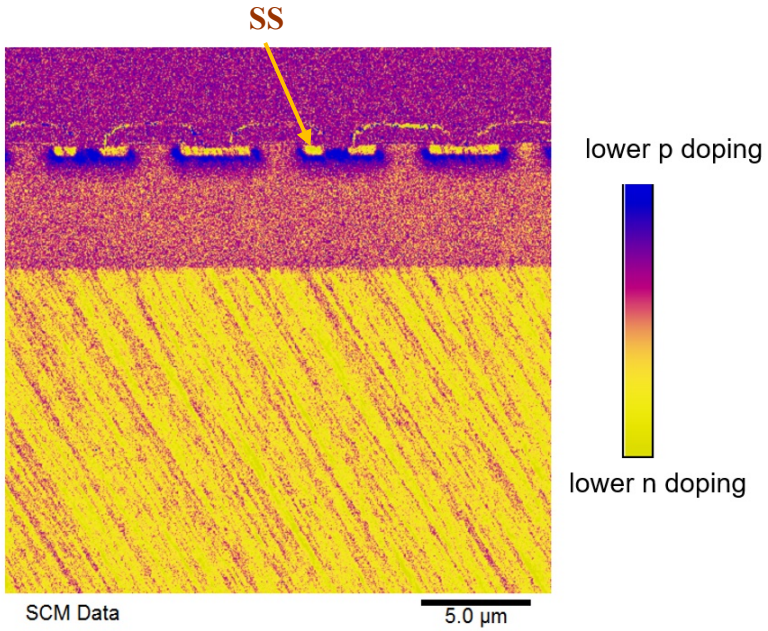


Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

a **(SS) second source region**;

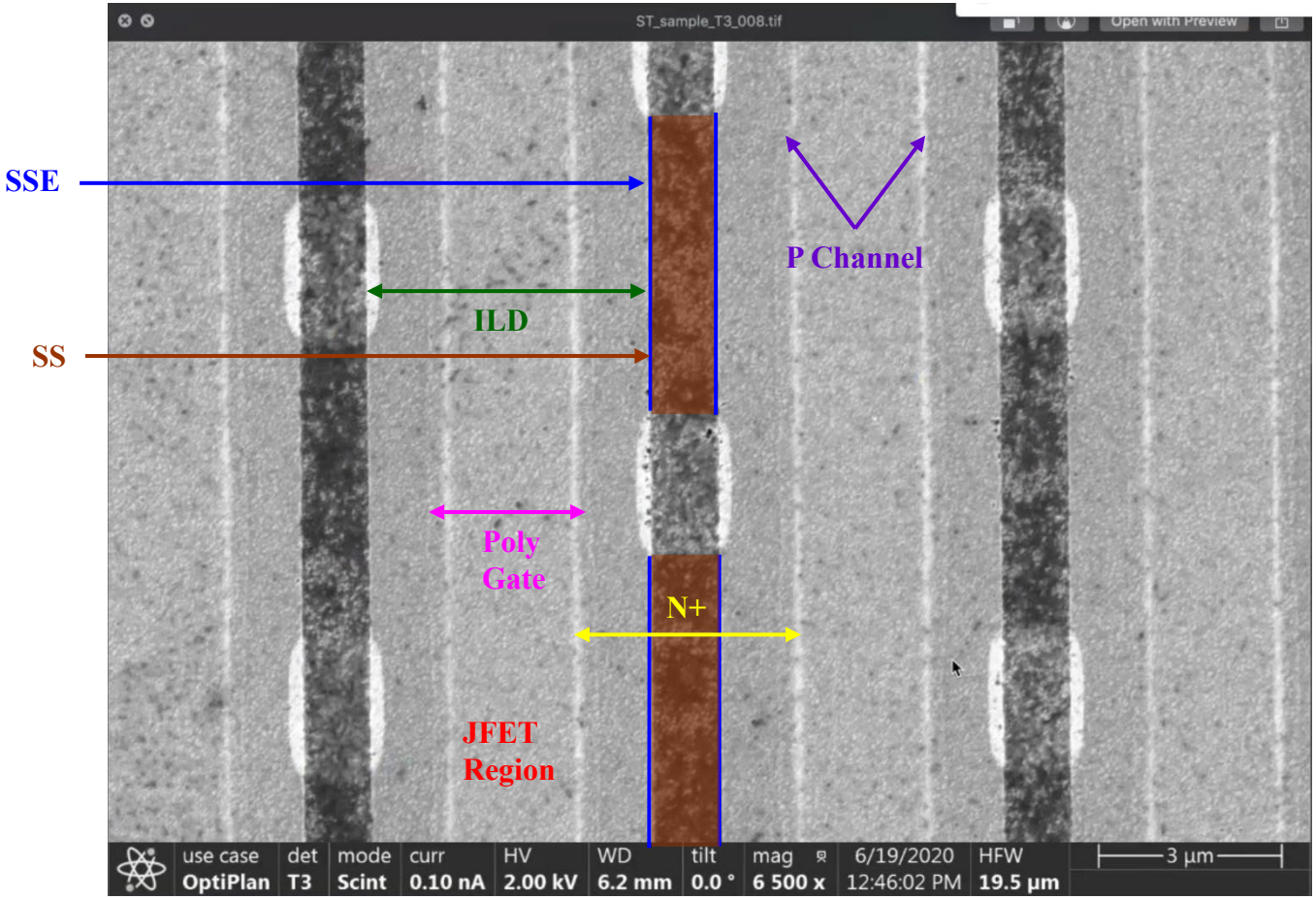




Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

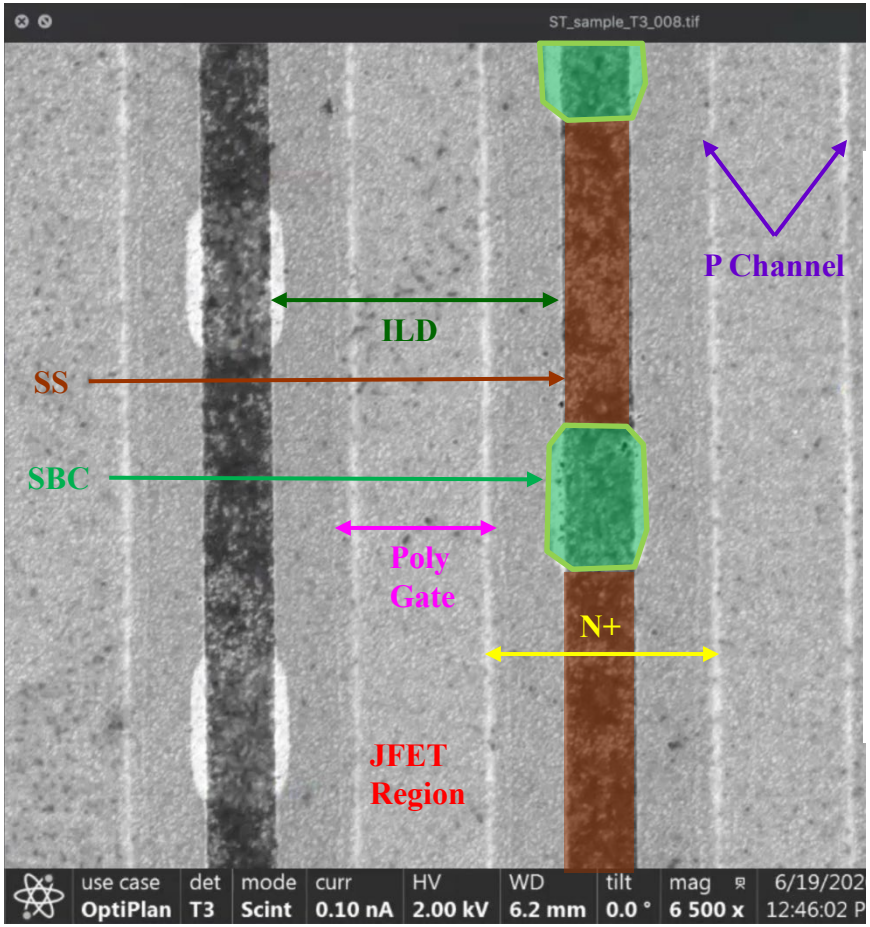
a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;

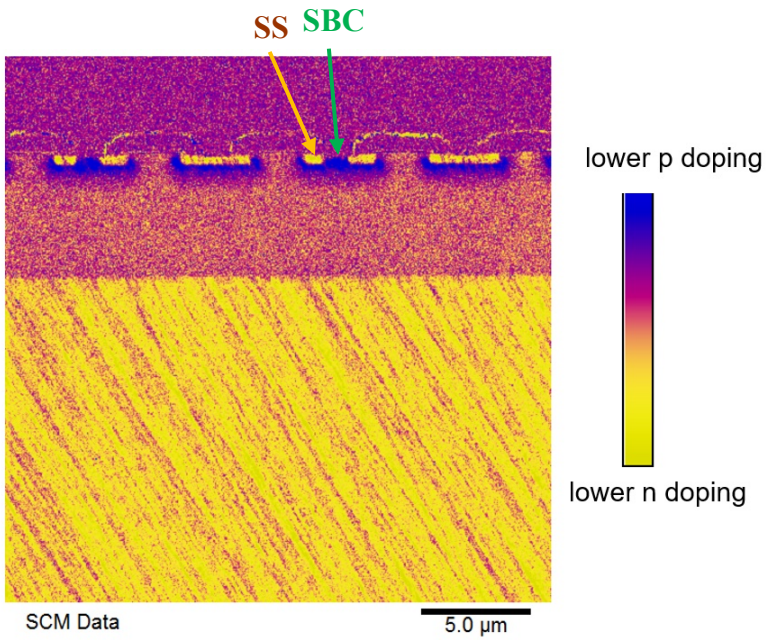


Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**,

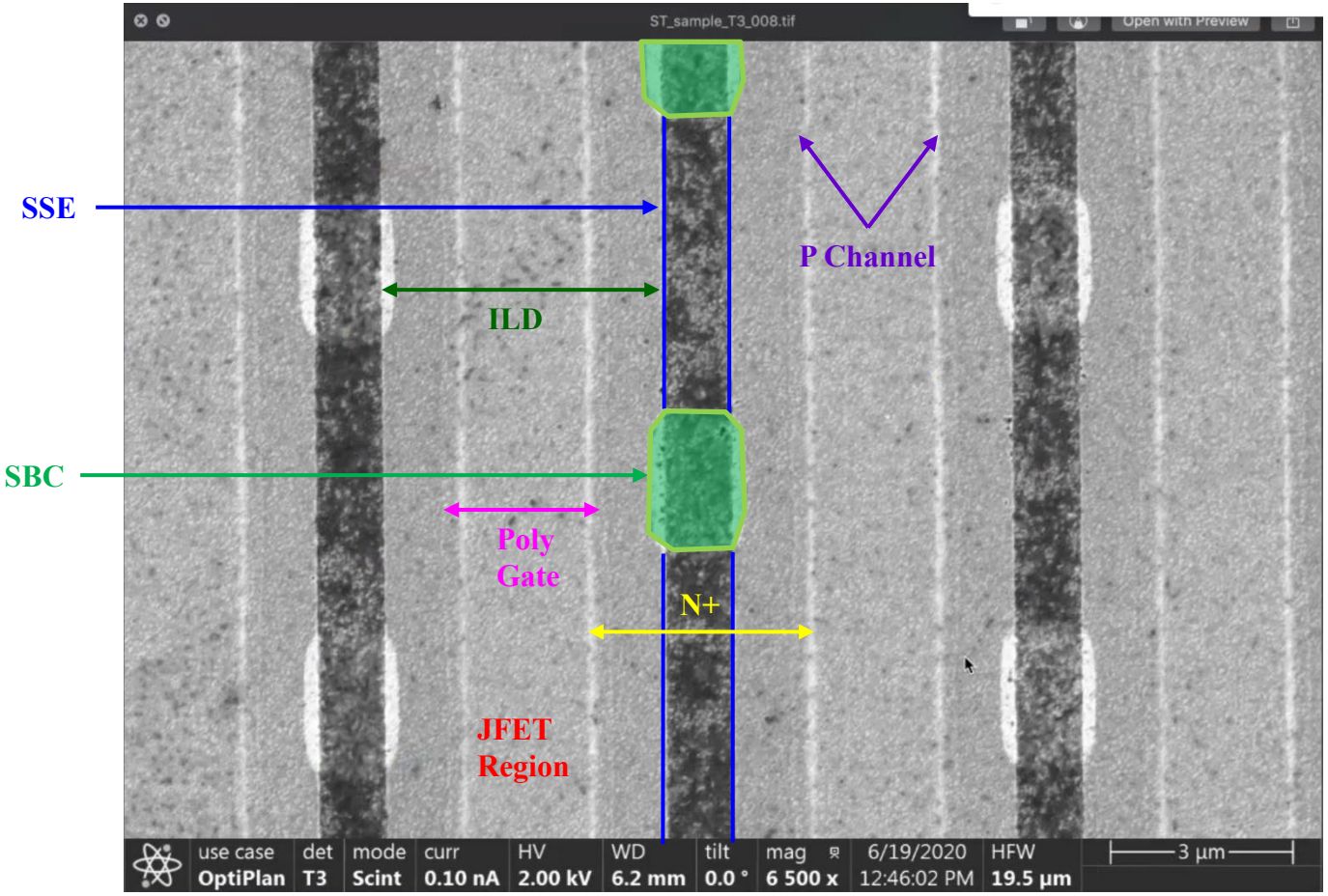




Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

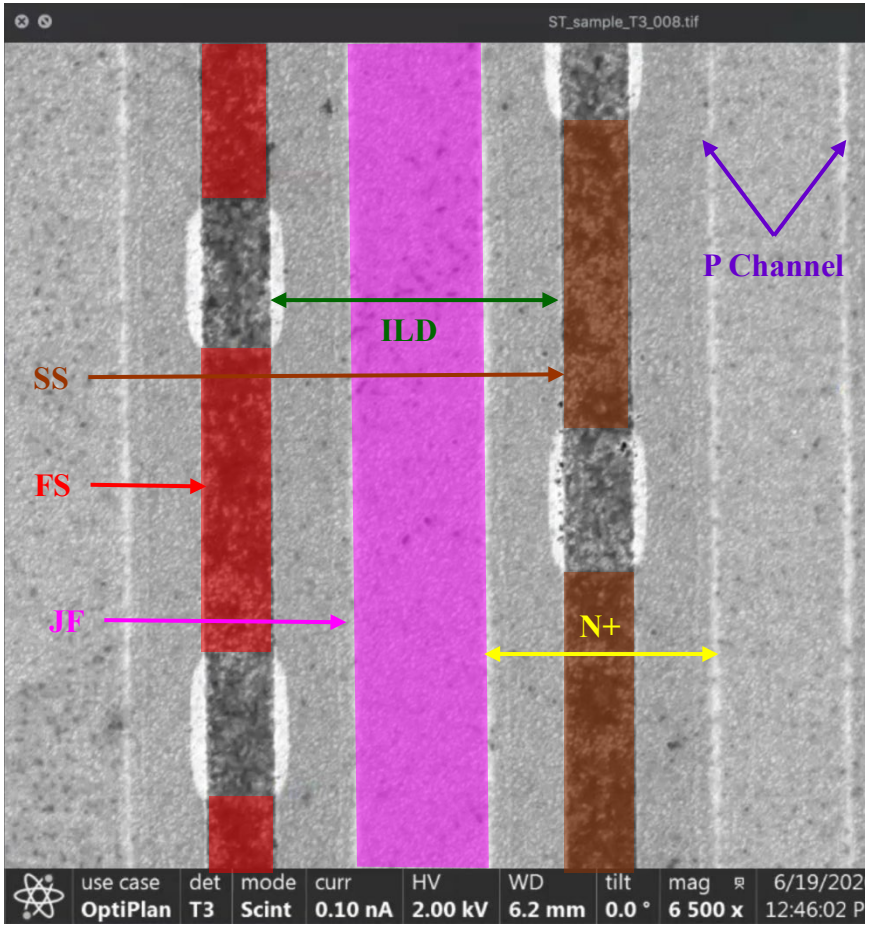
(SBC) each of the plurality of second base contact regions being spaced apart from each other in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and

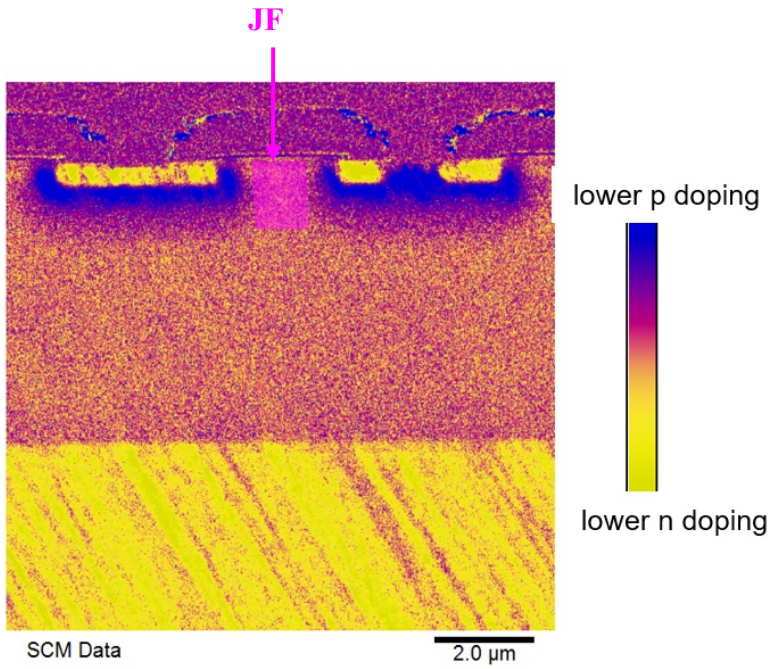


Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

a **(JF) JFET region defined between** the **(FS) first source region** and the **(SS) second source region**,

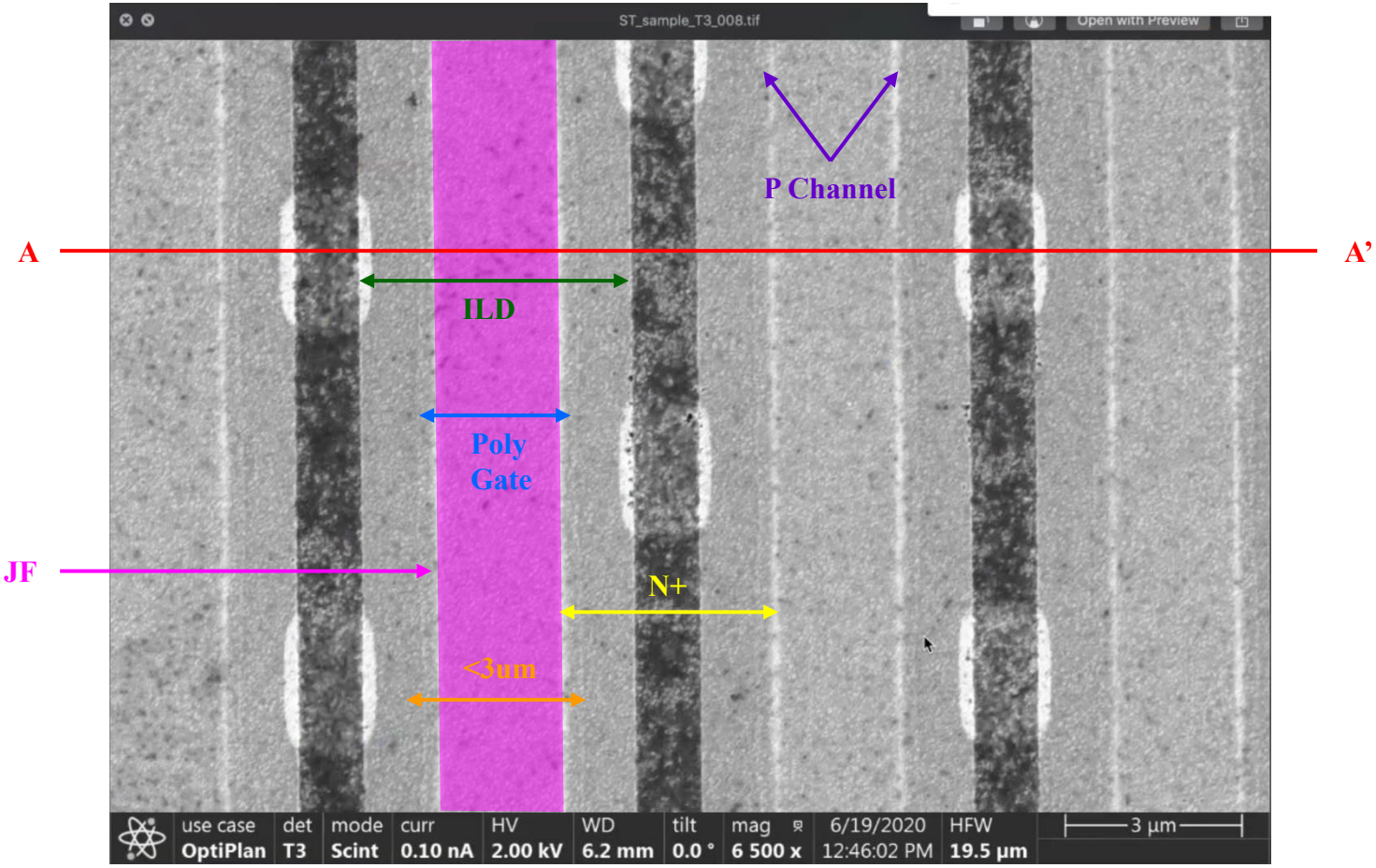




Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

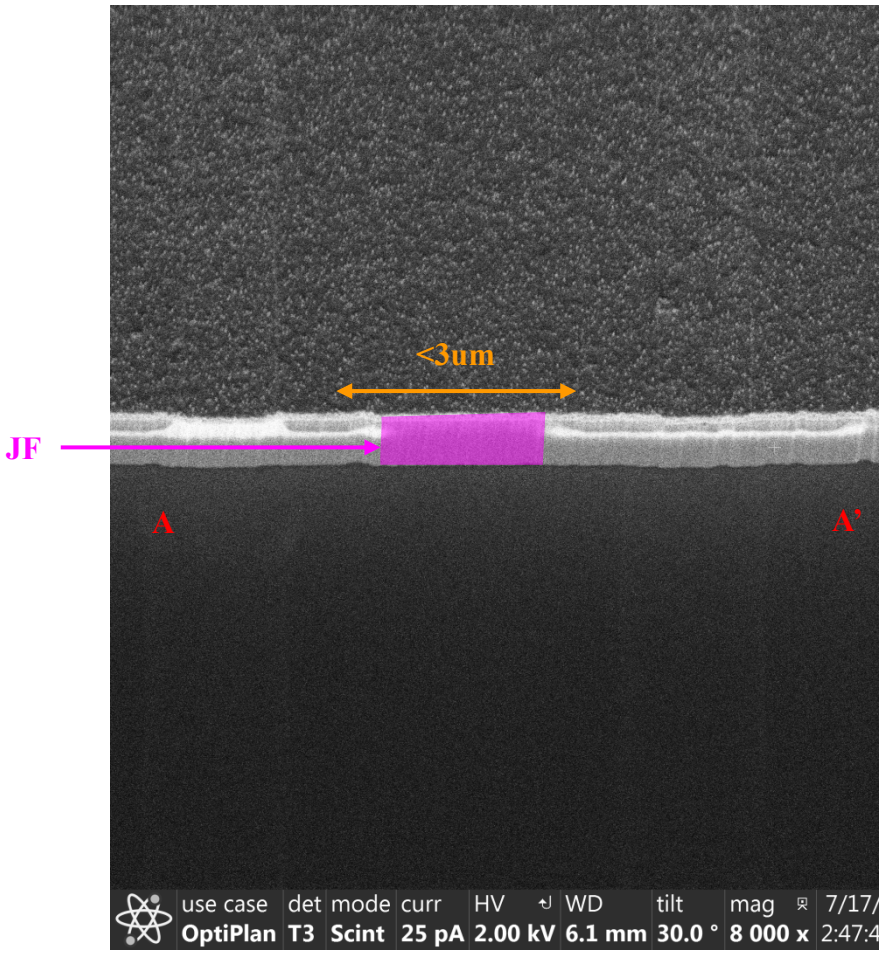
the **(JF) JFET region having a width less than about three micrometers**.

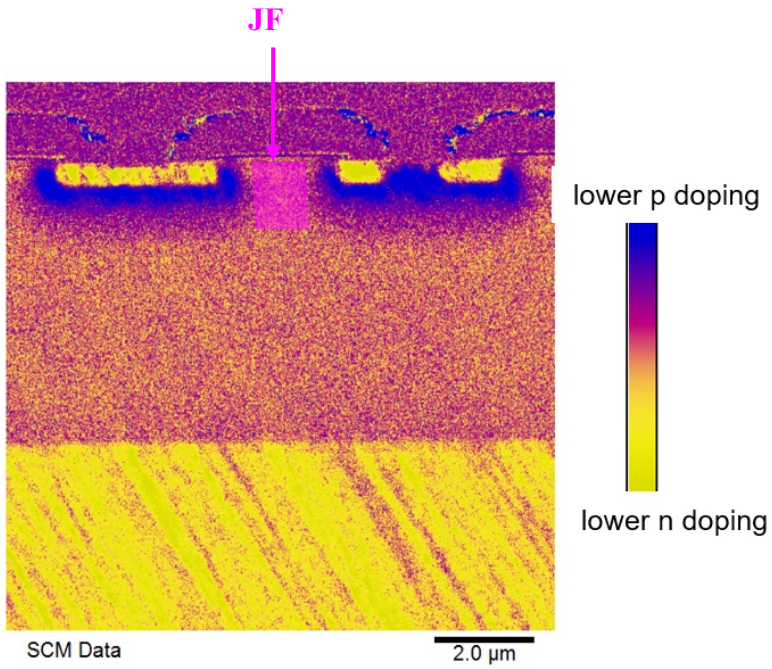


Note: The top down SEM SEPC above has been polished down to the silicon carbide.

Claim 9

the **(JF) JFET region having a width less than about three micrometers**.





Note: The cross-section **A-A'** of the previous page, SEM SEPC above has been polished down to the silicon carbide.